Negative-Bias Temperature Instability of GaN MOSFETs

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***Abstract*— We present a detailed study of the threshold voltage (V_T) instability of GaN n-MOSFETs under negative gate stress. We have investigated V_T shift, subthreshold swing (S) degradation and transconductance (g_m) degradation under negative gate voltage stress of different duration at different stress voltages and temperatures. We have found that as stress duration, voltage magnitude and temperature increase, V_T shift (ΔV_T) progresses through three regimes. Under low-stress, ΔV_T is negative and recoverable, which is a result of electron detrapping from pre-existing oxide traps. Under mid-stress, ΔV_T is positive and also recoverable. This appears to be due to temporary electron trapping in the GaN channel under the edges of the gate. For high-stress, there is an additional non-recoverable negative ΔV_T, which is consistent with interface state generation.**

I. Introduction

GaN high-electron-mobility-transistors (HEMTs) offer superior performance under high voltage, high temperature and high frequency operating conditions, which make them promising alternatives to silicon for future generation of power electronics [1]. For power switching applications, specifically, the GaN HEMT with an insulated-gate (MIS-HEMT) is the favored structure, because the addition of a gate insulator suppresses gate leakage and allows for enhancement-mode (E-mode) operation, both important for power switching devices [2]. However, introducing an insulating layer also brings in additional defects and trap states that can lead to severe device instabilities. For example, it has been reported that V_T instability in GaN MIS-HEMTs is much larger compared to GaN HEMTs [3]. This is a serious concern for depletion-mode (D-mode) devices when they need to be turned off, and for both D-mode and E-mode devices during OFF-state operation.

NBTI has been a critical reliability issue in MOSFETs made out of many material systems such as Si, SiC, and InGaAs. In Si p-MOSFETs, NBTI has been studied intensively since early 2000's after Nitrogen was introduced to CMOS processes. This is because it was found that Nitrogen enhances NBTI [4]. During NBTI, positive charge can be trapped at interface-states, in the oxide bulk or in near-interface defects (border traps) [5]. These trapped charge not only causes a negative V_T shift, but it also degrades channel carrier mobility through Coulomb scattering if it is close to the inversion layer [4], [6]. Under high stress, S degradation was also observed as a result of interface state generation [7]. Similar observations were made in SiC MOS capacitors, where a decrease in lifetime (partially recoverable) and increase in interface state density took place after negative gate voltage stress [8]. For III-V transistors, a study on ZrO_2/Al_2O_3/InGaAs MOSFETs showed that a combination of trap-discharge and interface degradation under NBTI caused a negative V_T shift [9], which is also consistent with findings in Si MOSFETs.

Compared to other material systems, the current understanding of NBTI in GaN MIS-HEMTs is very limited. This is mainly due to the multi-layered gate stack with multiple interfaces that present many opportunities for trapping with complex dynamics [10]–[12]. Progress can be made by studying simpler structures that isolate the roles of different layers and interfaces. The GaN MOSFET, in particular, allows us to isolate the roles of the gate dielectric and its interfaces. This structure on its own is also a strong candidate for power electronic applications [2], [13].

A recent publication has compared the bias temperature instabilities of GaN HEMT, GaN MIS-HEMT, and E-mode GaN MOSFET structures [14]. It was found that under negative voltage stress, while GaN HEMTs and MIS-HEMTs showed a negative V_T shift, which is the typical behavior in other material systems, E-mode GaN MOSFETs showed a positive V_T shift [14]. It was suggested in this study that this positive shift is a result of gate injection and subsequent electron trapping in the recessed GaN region. However, these observations and conclusions were made based solely on I_D-V_{GS} and C-V characterization at room temperature. A more comprehensive analysis is needed to provide a solid understanding of the mechanisms behind NBTI in GaN MOSFETs.

In this study, we examine the effect of NBTI in GaN MOSFETs with a SiO_2/Al_2O_3 composite dielectric. We present a detailed analysis of the dynamics of V_T, S and g_m before, during and after negative gate stress under a wide range of conditions. The results suggest a rich collection of physical mechanisms that affect V_T and other figures of merit in different ways.

II. Experimental

A. Device structure

The cross section of the device under study is sketched in Fig. 1 (not to scale). This is a simple AlGaN/GaN recessed-gate structure in which the AlGaN layer is removed from the intrinsic gate region. The gate stack consists of EOT=40 nm composite SiO_2/Al_2O_3 dielectric (Al_2O_3 next to the GaN

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channel). The devices used in this work have channel width/length of 100 µm/1 µm. Standard figures of merit for these devices in the saturation regime (V_{DS} = 10 V) are: V_{Tsat} ~ -0.8 V, S ~ 188 mV/dec, and g_{m_max} ~ 28 mS/mm.

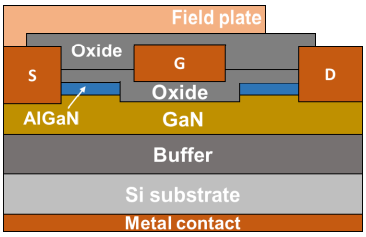

Figure 1. GaN MOSFET structure studied in this work.

In this work, we characterize the impact of negative gate bias stress on device behavior through figures of merit defined in the linear operating region (at V_{DS} = 0.1 V). In particular, we focus our interest on the stability of V_T (defined at drain current I_D = 1 µA/mm), S (defined at I_D = 0.1 µA/mm) and the maximum transconductance ($g_{m,max}$). Virgin devices used in this work exhibit values of V_T = 0.21 V with a standard deviation of 0.06 V, S = 157 mV/dec, and $g_{m,max}$ = 0.85 mS/mm.

B. *Experimental flow*

In this study we use a benign characterization scheme that parallels the one utilized in our earlier positive-bias temperature instability (PBTI) studies [15]. It is worth mentioning that $g_{m,max}$ measurements for NBTI need extra care, as compared to PBTI, because a positive gate voltage above V_T is needed to extract $g_{m,max}$. This by itself results in a V_T shift, affects the extracted value of g_m and complicates further experiments on the same device. To minimize this effect, we first calibrate the gate voltage needed to extract $g_{m,max}$, which is found to be ~ 1.5 V above V_T. We find that this point is stable after low- and mid-tress conditions. Then, to extract $g_{m,max}$ in stress experiments of this kind, we use V_T + 1.5 V as the upper bound of an I_D-V_{GS} sweep. We verified this approach by carrying out parallel sets of stress experiments on identical samples up to $V_{GS,stress}$=-30 V for 10^3 seconds. In one case, only V_T and S measurements were performed. In the second one, $g_{m,max}$ was additionally extracted. The difference in the measured values of V_T and S in these paired sets of experiments was less than 5%.

For harsh stress conditions, as we show below, there is non-recoverable damage in the device after stress. In particular, there is a significant S increase. This implies that a larger V_{GS} sweep range is needed to obtain $g_{m,max}$. This is a problem because it causes a significant change in the extracted figures of merit. As a solution, in harsh stress experiments, we use two identical devices for each stress period. From one of them we extract V_T and S using short I_D-V_{GS} sweeps, from the second one we extract $g_{m,max}$ using an extended V_{GS} range as needed.

In order to further understand the impact of electrical stress on the electrostatics of the device we have also performed C-V characterization. In these measurements, we measure either the gate voltage dependence of the capacitance between the gate and source/drain while keeping the body floating (C_{G_SD}-V_G), or the capacitance between the gate and source/drain/body (C_G-V_G).

III. Results and Discussion

Our study shows a peculiar three-regime behavior of V_T and S for GaN MOSFETs under negative gate bias stress. The progression of this behavior can be seen in Fig. 2. We apply gate stress, $V_{GS,stress}$= -10 V for 10^4 sec at T = 175°C. For short stress time (t_{stress}), ΔV_T is negative. As t_{stress} increases, ΔV_T becomes positive and continues to increase with t_{stress} until t_{stress} ~ 100 s. Beyond this point, ΔV_T starts to decrease and eventually becomes negative again. After the removal of stress, a benign thermal detrapping step (TD) reveals a residual negative ΔV_T (open symbol at right) that is not recoverable. In the course of the same experiment, the subthreshold swing S increases with stress time, then peaks and starts recovering. At the end of the experiment, after thermal detrapping, a residual degradation of S is left. Our study focuses on each of the three regimes in detail.

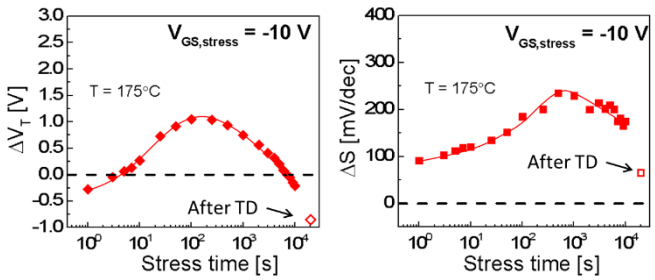

Figure 2. ΔV_T and ΔS as a function of stress time for $V_{GS,stress}$ = -10 V at 175°C. ΔV_T and ΔS taken 1 s after stress removal using short I_D-V_{GS} sweeps. The open symbols at the end indicate final ΔV_T and ΔS after a benign thermal detrapping (TD) step.

A. *Regime 1 (low-stress)*

For low $|V_{GS,stress}|$, low T (room temperature or below) and short t_{stress}, ΔV_T is negative and increases with time and ΔS is negligible. This is seen in Fig. 3 where we show ΔV_T and ΔS as a function of t_{stress} for $V_{GS,stress}$ = -1, -3 and -5 V, up to t_{stress} = 10^4 sec at room temperature. The recovery of ΔV_T and ΔS after removal of stress are also shown on the right. During the stress period, $|\Delta V_T|$ increases with $V_{GS,stress}$ and t_{stress} but eventually saturates. For $V_{GS,stress}$ = -5 V, ΔV_T peaks and then turns around after t_{stress} = 1000 s, which indicates the onset of regime 2. For all three stress voltages, we see minimal ΔS. During ΔV_T recovery, for $V_{GS,stress}$ = -1 and -3 V, V_T completely recovers at ~ 1000 s. For $V_{GS,stress}$ = -5 V, V_T first recovers and then overshoots at t_{stress} = 300 sec, and eventually recovers completely after thermal detrapping. We also find that the change in $g_{m,max}$ is also minimal and completely recoverable (not shown).

In Fig. 4, we compare I_D-V_{GS} and C_G-V_G characteristics before stress, after stress and after thermal detrapping for a device subjected to -1 V stress for 10^4 s at RT. We see a simple parallel V_T shift that completely recovers.

Fig. 5 shows the stress time evolution of $|\Delta V_T|$ in a log-log plot at three different temperatures and three different stress voltages. In all cases, the data follow a power law with

exponent n = 0.28 to 0.4 and a weak temperature dependence. This suggests that the process takes place mostly through tunneling.

All our observations are consistent with electron detrapping from oxide traps close to the oxide/semiconductor interface and subsequent retrapping when the device is brought to rest [12]. This is in essence the inverse process of the positive-bias temperature instability (PBTI) studies carried out earlier in these same devices [15]. Similar NBTI behavior has been reported in Si [16], [17] and SiC MOSFETs [18].

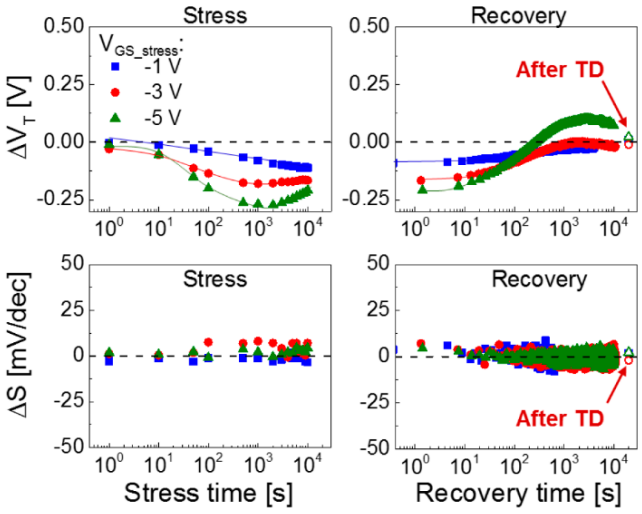

Figure 3. ΔV_T and ΔS as a function of stress time (extracted 1 s after removal of stress) and during subsequent recovery, for $V_{GS,stress}$ = -1, -3 and -5 V at RT. Open symbols at the end of recovery represent ΔV_T and ΔS after thermal detrapping (TD).

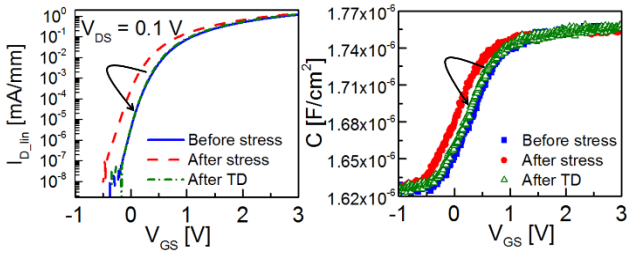

Figure 4. I_D-V_{GS} and C_G-V_G characteristics of a device before stress, after stress and after thermal detrapping (TD), for $V_{GS,stress}$ = -1 V, t_{stress} = 10,000 s at RT.

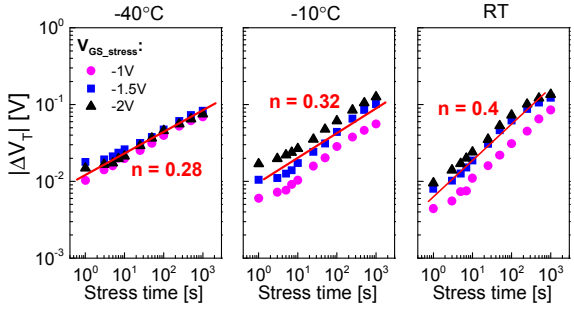

Figure 5. Stress time evolution of $|\Delta V_T|$ for $V_{GS,stress}$ = -1 to -2 V, at -40°C, -10°C and RT.

B. Regime 2 (mid-stress)

As stress increases, (higher $V_{GS,stress}$, longer t_{stress}, or higher T), the initial negative ΔV_T becomes positive. Fig. 6 (a) shows an example of this transition with $V_{GS,stress}$ = -5 V at -45°C, RT and 125°C. As we increase t_{stress} and T, the initial negative ΔV_T becomes positive and an increase in S is also observed. In addition, ΔV_T and ΔS are well correlated throughout the stress and recovery periods, as shown in Fig. 6 (b).

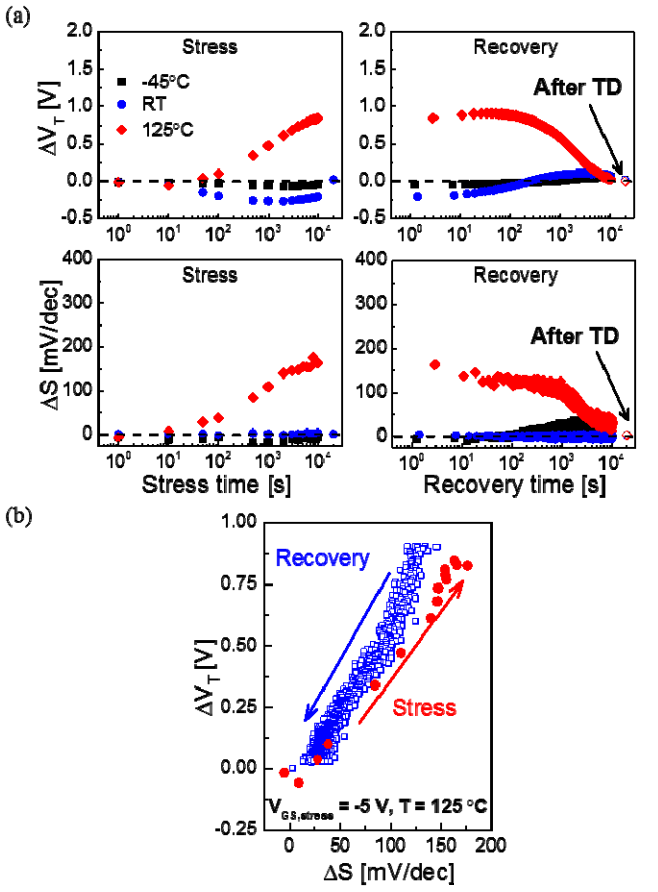

Figure 6. (a) ΔV_T and ΔS as a function of stress time (extracted 1 s after removal of stress) and recovery time, for $V_{GS,stress}$ = -5 V at -45°C, RT and 125°C. Recovery is traced after 10000 s stress using short I-V sweeps. (b) Correlation of ΔV_T and ΔS during stress and recovery for $V_{GS,stress}$ = -5 V at 125°C. ΔV_T and ΔS are linearly correlated.

Fig. 7 shows the stress time evolution of ΔV_T, ΔS, $\Delta g_{m,max}$ for $V_{GS,stress}$ = -10 to -20 V at RT, 75, 100 and 125°C. In addition to the positive ΔV_T and the accompanying ΔS, there is also a minor $g_{m,max}$ drop. All three parameter shifts are enhanced by higher $V_{GS,stress}$ and T. In addition, ΔV_T and ΔS both follow a log-time dependence with a T-independent slope. After thermal detrapping, ΔV_T, ΔS and $\Delta g_{m,max}$ mostly recover, except for $V_{GS,stress}$ = -20 V at T = 125°C, where residual ΔV_T (negative), ΔS, and $\Delta g_{m,max}$ are observed. This residual permanent degradation indicates a transition to regime 3.

The positive ΔV_T in regime 2 is in opposite direction from what has been reported for NBTI in other material systems, but it is consistent with a recent study on a similar recessed gate E-mode GaN MOSFET structure [14]. In order to better

understand this positive V_T shift, we also measure the C_{G_SD}-V_G characteristics before and after stress as shown in Fig. 8. This reveals the appearance of a temporary charge buildup around threshold after stress that disappears with subsequent thermal detrapping.

These observations suggest that the increase in S and the shift in V_T in Figs. 6 and 7 could arise from field-induced electron trapping in the GaN channel under both edges of the gate on the source and drain sides [19]. Electron trapping in the channel can take place under high reverse electric-field when electrons tunnel from the valence band to trap states in the GaN channel in a process sometimes referred to as Zener trapping. This is sketched in Fig. 9 (a) [18]. A process of this kind under the edge of the field plate has been shown to result in total current collapse in GaN MIS-HEMTs under high-voltage OFF-state stress [18].

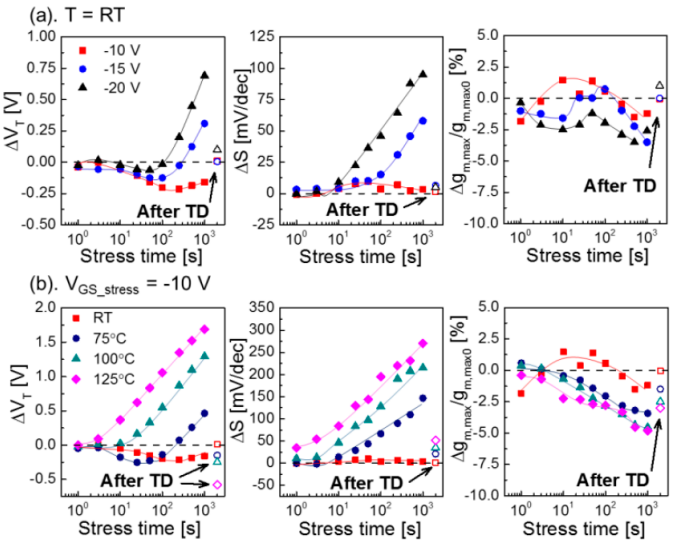

Figure 7. Stress time evolution of ΔV_T, ΔS and $\Delta g_{m,max}$ for (a) $V_{GS,stress}$ = -10, -15 and -20 V at RT, and (b) $V_{GS,stress}$ = -10 V at RT, 75°C, 100°C, 125°C.

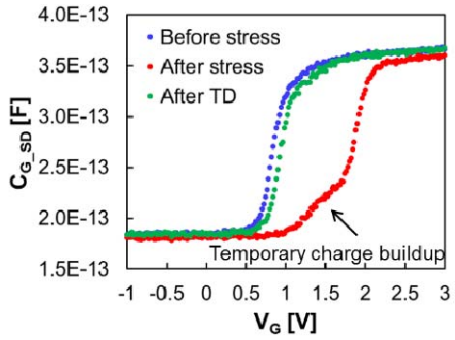

Figure 8. C_{G_SD} -V_G characteristics before and after $V_{GS,stress}$ = -20 V at RT for 1,000 s and after subsequent thermal detrapping. The body is grounded.

In the present work, under this hypothesis, high electron trapping lifts the bands up in the GaN channel effectively increasing the local hole concentration under both edges of the gate (Fig. 9 (b), (c)). This shifts V_T positive as well as increases the subthreshold swing. Both effects are temporary. As electrons detrap, the device eventually relaxes to its original state (Fig. 9 (c)). This trapping/detrapping process is possibly related to deep C traps with an energy level reported to be 2.85 eV from the conduction band edge of GaN [20]. This mechanism runs in parallel with that of regime 1 and eventually overwhelms it. It is completely recoverable.

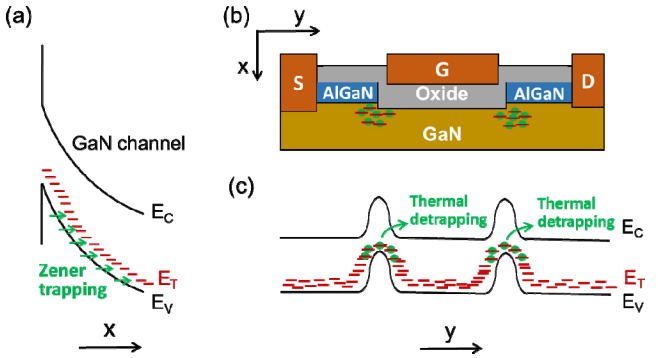

Figure 9. (a) Zener trapping mechanism as suggested in [18]. Electrons tunnel from the valence band into defect states (ET) under high vertical electric field in the GaN channel caused by high reverse bias stress. (b) Electron are trapped in the GaN channel under the source and drain edges of the gate. (c) High electron trapping lifts up the energy bands at the surface of the GaN channel shifting the threshold voltage positive under the edges of the gate and effectively increasing the local hole concentration. After stress removal, electron detrapping takes place through thermal processes.

C. *Regime 3 (high-stress)*

For harsh stress conditions, there is an additional negative V_T shift that is non-recoverable, as seen in Fig. 2 and Fig. 7. In the course of a stress experiment, this permanent degradation is often masked by regime 2 but it becomes evident after thermal detrapping. This non-recoverable negative V_T shift is accompanied by a non-recoverable increase in S and a permanent decrease in $g_{m,max}$. This degradation pattern becomes more severe with higher t_{stress} and $V_{GS,stress}$ as shown in Fig. 10. It is also accelerated by T, as shown in Fig. 11.

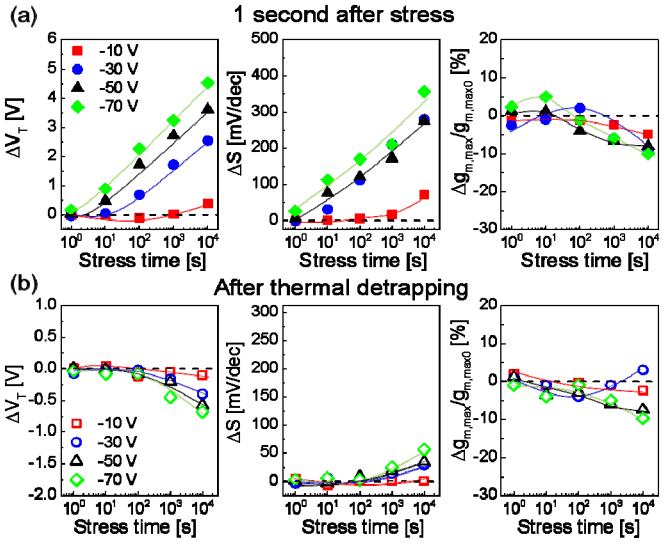

Figure 10. ΔV_T, ΔS and $\Delta g_{m,max}$ (a) immediately after stress at RT for $V_{GS,stress}$ = -10, -30, -50 and -70 V, and (b) after thermal detrapping performed along the experiment.

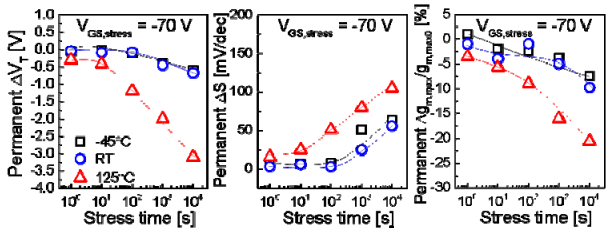

Figure 11. ΔV_T, ΔS and $\Delta g_{m,max}$ after thermal detrapping at different times in stress experiments. $V_{GS,stress}$ = -70 V and T = -45°C, RT and 125°C.

In addition, we also see that the permanent shift in V_T, ΔS and $\Delta g_{m,max}$ are well correlated as indicated in Fig. 12. In Fig. 13, we see the changes in I_D-V_{GS} and C_G-V_G characteristics. After stress and thermal detrapping, there is a prominent negative threshold voltage shift and degradation of S that correlates with a softening of the C-V characteristics around threshold. This is all consistent with the formation of interface states as a result of, perhaps, broken H bonds at the oxide/semiconductor interface. Similar phenomena are well documented in high-k/Si [21], [22] and Al_2O_3/InGaAs MOSFETs [23].

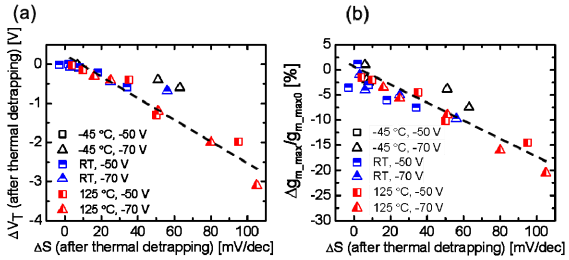

Figure 12. Correlation of (a) permanent ΔV_T and permanent ΔS and (b) permanent $\Delta g_{m,max}$ and permanent ΔS for $V_{GS,stress}$ = -50 and -70 V at different T.

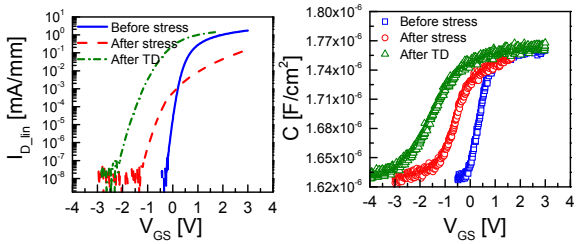

Figure 13. I_D-V_{GS} and C-V characteristics of a device before stress, after stress and after thermal detrapping (TD), for $V_{GS,stress}$ = -70 V for t_{stress}=500 s at 125°C.

IV. Conclusions

We identified three degradation mechanisms that are responsible for NBTI in oxide/GaN MOSFETs. Under low-stress, recoverable electron detrapping from pre-existing oxide traps close to the oxide/GaN interface takes place, which shifts V_T negatively. Under mid-stress, an additional transient positive V_T shift is observed that is accompanied by a temporary increase in S. This appears to be caused by electron trapping in the GaN channel under the edges of the gate. Under high-stress conditions there is also a permanent negative V_T shift and permanent degradation in g_m and S. This is consistent with interface state generation. These studies should be instrumental in understanding the more complex instability issues of GaN MIS-HEMTs.

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